

CLAIMS

What is claimed is:

1. A method of forming an interconnect conductor on a semiconductor wafer, the method comprising:
 - 5 forming a trench within a first dielectric layer on the semiconductor wafer;
filling the trench by electroplating copper simultaneously with a metal dopant to form a doped copper layer;
reducing the top level of the doped copper layer to form a planarized surface level with the surface of the first dielectric layer; and
 - 10 annealing the doped copper under annealing conditions sufficient to drive the metal dopants to form a metal dopant capping layer at the planarized top surface of the doped copper layer.
2. The method of forming an interconnect as recited in claim 1, wherein the metal dopants comprise Sn.
- 15 3. The method of forming an interconnect as recited in claim 1, wherein the metal dopants comprise one of In and Pb.
4. The method of forming an interconnect as recited in claim 1, wherein the metal dopants comprise a metal with a surface energy less than about 1830 mJ/m^2
5. The method of forming an interconnect as recited in claim 1, wherein the
20 metal dopants concentration is adjusted by adjusting the concentration level of a dopant salt in a Cu-plating electrolyte bath.
6. The method of forming an interconnect as recited in claim 1, wherein the annealing conditions comprise a temperature of 150 to 400C.
7. The method of forming an interconnect as recited in claim 1, wherein the
25 annealing conditions comprise a temperature of 150 to 400C and a duration of about 5min to 180min.

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8. The method of forming an interconnect as recited in claim 1, wherein the metal dopant capping layer extends from the planarized surface to a depth in the range from about 5 to 100 Angstroms.

5 9. The method of forming an interconnect as recited in claim 1, wherein the metal dopant capping layer extends from the planarized surface to a depth of 10 to 30 Angstroms.

10. The method of forming an interconnect as recited in claim 1, wherein the doped copper layer comprises less than 5 % metal dopants.

10 11. The method of forming an interconnect as recited in claim 1, further comprising a pre CMP annealing of the doped copper layer before reducing the top level of the doped copper layer to form a planarized surface.

12. The method of forming an interconnect as recited in claim 11, wherein the pre-CMP annealing step is performed at a temperature of less than 100 C.

15 13. The method of forming an interconnect as recited in claim 1, wherein the doped copper layer comprises between 0.5 and 2 % metal dopants.

14. The method of forming an interconnect as recited in claim 1, wherein the annealing conditions comprise a temperature of 250 to 350C.

15 15. A semiconductor interconnect structure, the interconnect structure comprising:
20 a first dielectric having an inlaid metal interconnect line formed in it and a planarized surface formed at the top of the dielectric and the metal interconnect line, wherein a metal coating film is formed beneath the planarized surface directly on the inlaid metal line.

25 16. The semiconductor interconnect structure of claim 15 wherein the metal film comprises Sn.

17. The semiconductor interconnect structure of claim 15 wherein the thin metal film comprises one of In and Pb.

18. The semiconductor interconnect structure of claim 15 wherein the metal film extends from the planarized surface to a depth of 5 to 100 Angstroms.

19. The semiconductor interconnect structure of claim 15 wherein the metal film extends from the planarized surface to a depth of 10 to 30 Angstroms.

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